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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/837,517	04/19/2001	Nobuo Suzuki	107317-00028	8208

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EXAMINER	
DANIELS, ANTHONY J	
ART UNIT	PAPER NUMBER
2622	

DATE MAILED: 06/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/837,517	SUZUKI ET AL.	
	Examiner	Art Unit	
	Anthony J. Daniels	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-12,15,16,19,20,23 and 24* is/are allowed.

6)☒ Claim(s) *1,2,4,5,17 and 18* is/are rejected.

7)☒ Claim(s) *3,6,21 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment, filed 4/10/2006, has been entered and made of record. Claims 1-24 are pending in the application.

Response to Arguments

2. Applicant's remarks regarding the Beiley reference used in the rejection of claim 1 have been considered. Examiner recognizes the deficiencies of Beiley et al. and has used the Kijima et al. and Miyamoto to cure those deficiencies.

3. Applicant's arguments, in regard to claim 3 and the Kijima reference, have been fully considered and are persuasive. Claim 3 is now objected to as being dependent on a rejected base claim.

4. Applicant's arguments filed 4/10/2006 have been fully considered but they are not persuasive.

As to applicant's arguments regarding the Miyamoto reference, the examiner respectfully disagrees.

On p. 20, Lines 10 and 11, applicant states, "...Miyamoto is silent regarding when the flashing signal is provided..." As is stated in the office action on page 7 (see claim 4), it is inherent that the read out and reset signals are not operated when the flashing signal is provided. If this were not the case, only a fraction of the image signals would be flash illuminated, presenting uneven images as far as illumination. Thus, making the flash unfit for its intended purpose.

The examiner believes all arguments have been addressed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1,2,4,5,17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beiley et al. (US 20020085106) in view of Kijima et al. (US # 6,661,451) and further in view of Miyamoto (US 20030090575).

As to claim **1**, Beiley et al. teaches an electronic camera (Figure 4; [0043], Lines 6-8) that does not use a mechanical shutter ([0005], Lines 6-11; *{In [0005], Beiley et al. teaches that CMOS imagers typically do not use mechanical shutters. Furthermore, the operation of the invention would not function as disclosed if a mechanical shutter were employed.}*), comprising: a MOS type solid-state image pickup device (Figure 4, imager chip "400"); comprising: (i) a semiconductor substrate (*A semiconductor substrate is inherent in a CMOS chip.*), (ii) a number of photoelectric conversion elements formed in one surface of said semiconductor substrate in a matrix shape along a plurality of rows and columns (Figure 4, pixel array "408"), (iii) a switching circuit (Figure 1, circuitry outside photodiode "14") provided for each photoelectric conversion element and electrically connected to an corresponding photoelectric conversion element (Figure 1), each switching circuit controlling generation of an output signal representative of charge accumulated in said corresponding photoelectric conversion element and drainage of said charge ([0022], [0023], Lines 1,2) , (iv) a row selection signal line disposed for each photoelectric conversion element row and electrically connected to corresponding switching

circuits (Figure 1, row signal "48"; "bit line"), each row selection signal line being supplied with a row selection signal for controlling generation of said output signal ([0022], Lines 5-7), (v) a plurality of output signal lines each of which is corresponded to at least one pixel column and on each of which said output signal is generated (*This is an inherent feature in CMOS imagers.*), (vi) a reset signal line disposed for each photoelectric conversion element row and electrically connected to corresponding switching circuits, each reset signal line being supplied with a reset signal for controlling drainage of said charges (Figure 1, reset signal "20"; [0023]), (vii) a readout row-shifter for sequentially supplying said row selection signal to each row selection signal line (Figure 4, row decoder "414"; [0048]), (viii) a reset row-shifter for sequentially supplying said reset signal to each reset signal line (Figure 4, row decoder "414"; [0048]), and (ix) an output device electrically connected to each output signal line for sequentially generating and outputting image signals representative of said output signals (Figure 4, column decoder "410" and A/D converter "420"); an image signal processor for generating image data based on said image signals output from said MOS type solid-state image pickup device (Figure 4, column decoder "410"); a moving image mode controller being connected to said MOS type solid-state image pickup device for continually controlling operation of said MOS type solid-state image pickup device, said moving image mode controller makes said MOS type solid-state image pickup device repeat (a) an image signal read operation of sequentially supplying said row selection signal from the readout row-shifter to a plurality of predetermined row selection signal lines for sequentially generating said output signals on each output signal line and (b) an electronic shutter operation of sequentially supplying said reset signal from the reset row-shifter to said reset signal lines corresponding to at least said rows to be subjected to said image signal

read operation for sequentially draining said charges accumulated in the photoelectric conversion elements ([0043], Lines 6-8; *{In [0043], Beiley et al. teaches the use of the imager chip in still and video image applications. Having disclosed this, it is inherent that the system of Beiley et al. repeatedly perform steps (a) and (b) when producing a video image.}*); and a correcting still image mode controller being connected to said MOS type solid-state image pickup device for controlling operation of said MOS type solid-state image pickup device in place of said moving image mode controller (Figure 4, row decoder "414"), an exposure time of each photoelectric conversion element is set equal to or shorter than a time duration including an issuance time of a flashing device operation signal and necessary for performing two image signal read operations before and after one electronic shutter operation (Figure 2, *{From the timing diagram of Figure 2, one image signal read operation (reading a plurality of pixels) would be much longer than the exposure time "204" of Figure 2, let alone two plus the time taken for the issuance of a flashing signal.}*), and after a lapse of said exposure time, said correcting still image mode controller makes said MOS type solid-state image pickup device perform an image signal read operation of sequentially supplying said row selection signal from the readout row-shifter to each row selection signal line for sequentially generating said output signals on each output signal line (Figure 2, [0039], [0040]). The claim differs from Beiley et al. in that it further requires that the system includes a still image indication signal generator for generating a still image indication signal for indicating image pickup of a still image, and a flashing device for emitting a flash in response to a reception of a predetermined signal, wherein a flashing device operation signal for operating said flashing device is made in the state that said readout row-shifter and said reset row-shifter are not operated.

In the same field of endeavor, Kijima et al. teaches a digital still/video camera (Figure 1) that takes either a still image or a video image dependent upon the status of an trigger which switches between a high speed image (video image) mode or high quality image (still image) mode (Abstract, Lines 4-7; Col. 3, Lines 16-25; 47-67). In light of the teaching of Kijima et al., it would have been obvious to one of ordinary skill in the art to include the trigger of Kijima et al. in the camera of Beiley et al., because an artisan of ordinary skill in the art would recognize that such a switch would allow the user to take a high quality image or sacrifice quality for high speed motion images.

In the same field of endeavor, Miyamoto teaches a digital camera that provides a flash illumination dependent upon a flash on/off switch (Figure 1, flash on/off "24"). In light of the teaching of Miyamoto, it would have been obvious to one of ordinary skill in the art to provide the flash signal of Miyamoto at a point where the readout and reset are not operated, because an artisan of ordinary skill in the art would recognize that this would allow all pixels of the image sensor to receive uniform illumination.

As to claim **2**, Beiley et al., as modified by Kijima et al. and Miyamoto, teaches an electronic camera according to claim 1, wherein the image signal read operation by said moving image mode controller and the image signal read operation by said correcting still image mode controller include (i) operation of sequentially supplying said row selection signal from the readout row-shifter to a plurality of predetermined row selection signal lines for sequentially generating said output signals on each output signal line in the unit of a photoelectric conversion element row and (ii) operation of sequentially draining said charges accumulated in each

photoelectric conversion element from which said output signal was generated, in the unit of a photoelectric conversion element row (Figure 2, [0039], [0040]).

As to claim **4**, Beiley et al., as modified by an electronic camera according to claim 1, further comprising: a non-correcting still image mode controller being connected to said MOS type solid-state image pickup device for controlling operation of said MOS type solid-state image pickup device in place of said moving image mode controller when said still image indication signal is made, wherein without making said flashing device operation signal, said non-correcting still image mode controller makes said MOS type solid-state image pickup device perform an image signal read operation of sequentially supplying said row selection signal from the readout row-shifter to each row selection signal line for sequentially generating said output signals on each output signal line (*It is inherent that during the read out and reset, the flash does not occur.*); and still image mode designating device for specifying beforehand a still image mode controller to be operated when said still image indication signal is made (see Kijima et al., trigger "46"; Abstract, Lines 6-8)

As to claim **5**, the limitations of claim 5 can be found in claim 2. Therefore, claim 5 is analyzed and rejected as previously discussed with respect to claim 2.

Note for claims 1, 2, 4 and 5: The functions of the correcting still image mode controller, the non-correcting still image mode controller, the moving image mode controller, and the still image mode controller are met by the references above. Therefore, the controllers are interpreted to be different signals that are applied to the imager chip "400" to perform these functions.

As to claim **17**, Beiley et al., as modified by Kijima et al. and Miyamoto, teaches an electronic camera according to claim 1, wherein said output device includes an analog output device for generating and outputting analog image signals representative of said output signals (see Beiley et al., Figure 4, column decoder "410"; [0047]) and a digital output device for receiving said analog image signals, converting said analog image signals into digital image signals, and outputting said digital image signals (see Beiley et al., Figure 4, A/D Converter "420"; [0047]).

As to claim **18**, the limitations of claim 17 can be found in claim 18. Therefore, claim 18 is analyzed and rejected as previously discussed with respect to claim 17.

5. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beiley et al. (US 20020085106) in view of Kijima et al. (US # 6,661,451) in view of Miyamoto (US 20030090575) and further in view of Hashimoto (US # 6,956,605).

As to claim **13**, Beiley et al., as modified by Kijima et al. and Miyamoto, teaches an electronic camera according to claim 1. The claim differs from Beiley et al., as modified by Kijima et al. and Miyamoto in that it further requires an auto iris for adjusting an amount of light incident upon said MOS type solid-state image pickup device, wherein said correcting still image mode controller in operation further performs an exposure amount adjustment operation of adjusting said auto iris to reduce a difference between exposure amounts to be caused by a difference between an exposure time under a control of said correcting still image mode controller and an exposure time under a control of said moving image mode controller.

In the same field of endeavor, Hashimoto teaches a CMOS image sensor that picks up images in two modes. The first is an addition mode where adjacent pixels are summed together to output more frames per second. The second is a high pixel count read out mode where a high-resolution image can be obtained. An iris is changed to half an exposure amount for the addition mode. The iris is at full exposure amount for the high pixel count read out mode (Col. 12, Lines 37-67; Col. 13, Lines 1-5). In light of the teaching of Hashimoto, it would have been obvious to one of ordinary skill in the art to include the auto-iris operation in the system of Beiley et al., as modified by Kijima et al. and Miyamoto, because an artisan of ordinary skill in the art would recognize that this would prevent an oversensitive signal from being obtained in the video mode of Beiley et al., as modified by Kijima et al. and Miyamoto (see Hashimoto, Col. 12, Lines 65-67; Col. 13, Lines 1-5).

As to claim **14**, the limitations of claim 14 can be found in claim 13. Therefore, claim 14 is analyzed and rejected as previously discussed with respect to claim 13.

Allowable Subject Matter

6. Claims 3,6,21 and 22 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: As to claims **3** and **6**, the prior art does not teach or fairly suggest a correcting or non-correcting still image mode controller that makes a MOS type solid-state image pickup device perform an image signal read operation following a electronic shutter operation and after a lapse in exposure time,

and thereafter a flashing device operation signal is made. Claims **21** and **22** are dependent upon claims 3 and 6, respectively.

7. Claim 7-12,15,16,19,20,23, and 24 are allowed.

The reasons for allowance can be found in the previous office actions.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony J. Daniels whose telephone number is (571) 272-7362. The examiner can normally be reached on 8:00 A.M. - 5:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc-Yen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AD
6/12/2006

TUAN HO
PRIMARY EXAMINER